**Multi-operand Floating-point Addition**

**——Synopsys**

## Contributions

1. Analyze the issues related to multi-operand addition.
2. Proposed the simultaneous addition of 3 operands.

## Requirements for multi-operand floating-point addition

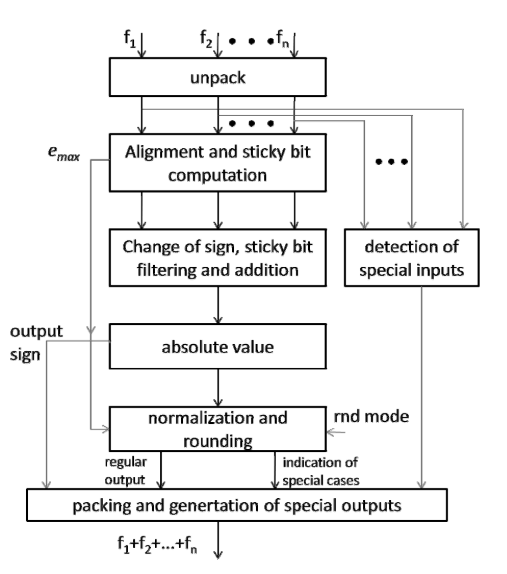
1. The output accuracy of the operator must be better than the accuracy of an equivalent network of 2-operand floating-point adders.
2. The delay for the solution should be better to or competitive with the network off 2-operand adders without excessive extra hardware.

## General issues in multi-operand addition

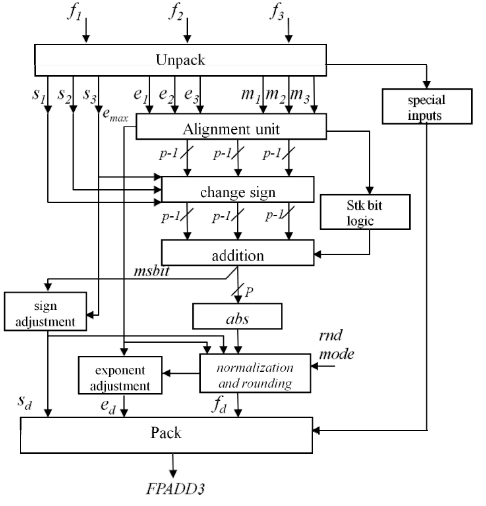
1. The internal precision used to execute multi-operand addition must be larger than the internal precision used in each 2-operand adder in a network.
2. The result of addition of floating point values using 2-operand floating-point adders depend on the sequence of operations (non-associative operation).

## Design of 3-operand floating point adder

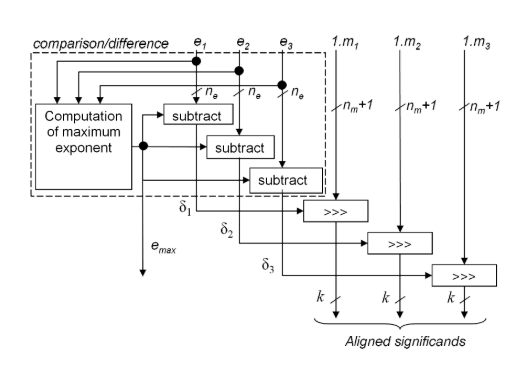
1. General architecture



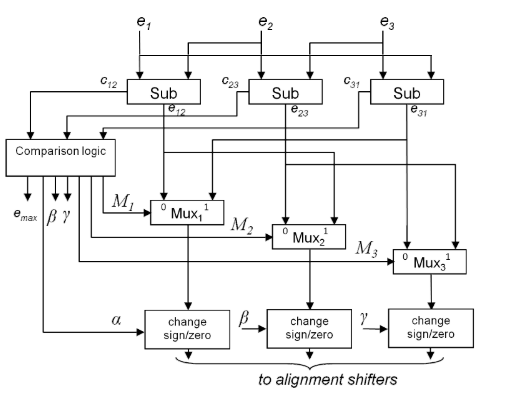
1. Proposed architecture



1. Alignment of significands

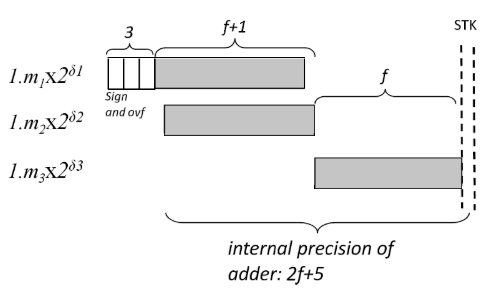


Previous

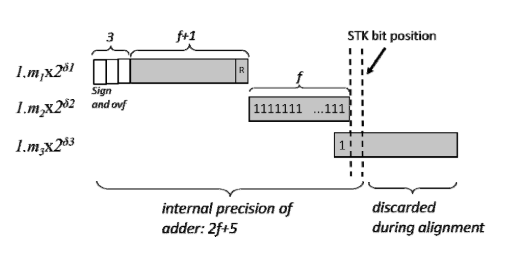


Modified

1. Internal precision



partial cancellation of operands



propagation of truncation errors

As a result of this discussion, an internal adder with 2f+

5 bits is required to implement a 3-operand floating point adder component.